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(Small Entity)

Docket No.
MAI1003

03/20/98 jc535 U.S. PTO

TO THE ASSISTANT COMMISSIONER FOR PATENTS

:itted herewith for filing under 35 U.S.C. 111 and 37 C.F.R. 1.53 is the patent application of:

. **Malcolm MacIntyre**

For: **CHIP SCALE PACKAGES**

Enclosed are:

- ☒ Certificate of Mailing with Express Mail Mailing Label No. **EH861754580US**
- ☒ **Three (3)** sheets of drawings.
- ☐ A certified copy of a application.
- ☒ Declaration ☒ Signed. ☐ Unsigned.
- ☒ Power of Attorney
- ☐ Information Disclosure Statement
- ☐ Preliminary Amendment
- ☒ **One** Verified Statement(s) to Establish Small Entity Status Under 37 C.F.R. 1.9 and 1.27.
- ☐ Other:

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Total Claims	14	- 20 =	0	x	$11.00	$0.00
Indep. Claims	2	- 3 =	0	x	$41.00	$0.00
Multiple Dependent Claims (check if applicable) ☐						$0.00
					BASIC FEE	$395.00
					TOTAL FILING FEE	$395.00

- ☐ A check in the amount of to cover the filing fee is enclosed.
- ☒ The Commissioner is hereby authorized to charge and credit Deposit Account No. **50-0230** as described below. A duplicate copy of this sheet is enclosed.
  - ☒ Charge the amount of **$395.00** as filing fee.
  - ☒ Credit any overpayment.
  - ☒ Charge any additional filing fees required under 37 C.F.R. 1.16 and 1.17.
  - ☐ Charge the issue fee set in 37 C.F.R. 1.18 at the mailing of the Notice of Allowance, pursuant to 37 C.F.R. 1.311(b).

Dated: **3/20/98**

H. Donald Nelson
Signature

H.Donald Nelson, Reg. No. 28,980

cc:

P01SMALL/REV06

CHIP SCALE PACKAGES

Donald Malcolm MacIntyre

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates generally to flip chip packaging technology and even more specifically, this invention relates to chip scale flip chip packaging technology for semiconductor die.

2. Discussion of the Related Art

Chip Scale Packages (CSP) for semiconductor die currently embody some form of solder ball or bump to attach the die to the next higher assembly in the total package. In the simplest form of a CSP, the CSP is a flip chip semiconductor die that has additional solder bumps to be connected to normal bond pads on a substrate which are used to wire bond interconnect to a package or substrate. The semiconductor die is inverted and the solder is reflow melted which structurally attaches the die to the metallized pads or to traces on the substrate.

The solder-bump flip-chip interconnection technology was initiated in the early 1960s to eliminate the expense, unreliability, and low productivity of manual wirebonding. The so-called controlled-collapse-chip connection C^4 or C4 utilizes solder bumps deposited on wettable metal terminals on the chip which are joined to a matching footprint of solder wettable terminals on the substrate. The upside-down

chip (flip chip) is aligned to the substrate and all joints are made simultaneously by reflowing the solder.

The most recent innovations to the flip chip technology involve the relocation of the solder ball/bump sites from the close pitch pads which are normally placed around the perimeter of the semiconductor die to an array located across the surface of the die. This is accomplished by creating new traces from the perimeter locations to the new array locations on top of a passivation layer. The passivation layer is typically a glass protective layer deposited on the surface of the die with openings to expose the bond pads or by adding an interposer connector, which is bonded to the existing pads and reroutes traces to the array. An interposer connector is a connector structure that is routed between two parts to be connected.

A current interposer connector process reroutes connectors to the pads by extending them into the space between adjacent die as created on the semiconductor wafer, laminating a piece of glass to either side of the wafer and then through a complex series of mechanical cutting, metal deposition and etching operations, the connectors to the pads are extended to the surface of the glass. This produces an array on the top of the glass sheet covering the die, which is in turn adhesively bonded to the passivation surface of the die. The advantage of this process and structure is that the glass sheet provides a protective surface for the delicate surface of the passivated die and allows some degree of differential expansion between the die surface and the array of solder balls due to the non rigid nature of the adhesive layer. The disadvantages are that the extension of the connectors to the pads on the wafer are difficult to implement

and often prevent the process from being possible, the glass cutting operation is costly and requires special equipment, the process is implemented on a completed semiconductor wafer which is very sensitive and costly and any error causes the entire wafer to be scrapped, and two sheets of glass are always required.

Therefore, what is needed is a chip scale flip chip process that is easy to implement, uses one glass sheet and is inexpensive.

SUMMARY OF THE INVENTION

According to the present invention, the foregoing and advantages are attained by a method and structure for a chip scale package formed by adhering a glass sheet having a pattern of holes matching a pattern of bond pads on a semiconductor wafer so that the pattern of holes on the glass sheet are over the pattern of bond pads on the semiconductor wafer. In one aspect of the invention, metallized pads are formed on the glass sheet adjacent to each hole and in one embodiment a metal trace is formed from each metallized pad on the glass sheet to the pad on the semiconductor wafer under the adjacent hole. In another aspect of the invention, a pad is formed on the glass sheet adjacent to each hole and the pad extends down the sides of the adjacent hole. In the second aspect, the hole is filled with a metal plug that electrically connects the pad on the glass sheet to the bond pad on the semiconductor wafer. In each aspect of the invention, a solder ball is formed on each pad on the glass sheet.

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The present invention is better understood upon consideration of the detailed description below, in conjunction with the accompanying drawings. As will become

readily apparent to those skilled in the art from the following description, there is shown and described embodiments of this invention simply by way of illustration of the best modes to carry out the invention. As will be realized, the invention is capable of other embodiments and its several details are capable of modifications in various obvious aspects, all without departing from the scope of the invention. Accordingly, the drawings and detailed description will be regarded as illustrative in nature and not as restrictive.

BRIEF DESCRIPTION OF THE DRAWINGS

The novel features believed characteristic of the invention are set forth in the appended claims. The invention itself, however, as well as a preferred mode of use, and further objects and advantages thereof, will best be understood by reference to the following detailed description of an illustrative embodiments when read in conjunction with the accompanying drawings, wherein:

Figure 1A shows a glass sheet that is to be used in the present invention;

Figure 1B shows the glass sheet shown in **Figure 1A** after being prepared to be adhered to a semiconductor wafer;

Figure 1C shows the glass sheet shown in **Figure 1B** adhered to a semiconductor wafer;

Figure 1D shows the completed glass sheet/semiconductor wafer structure;

Figure 2A shows a cross-section of a portion of the glass sheet shown in **Figure 1A**;

Figure 2B shows the portion of the cross-section of the glass sheet shown in **Figure 2A** with a hole formed in the glass sheet and a pad formed on the surface of the glass sheet;

Figure 2C shows the cross-section of the glass sheet shown in **Figure 2B** after the glass sheet has been adhered to a semiconductor wafer as shown in **Figure 1C**;

Figure 2D shows the glass sheet/semiconductor wafer structure as shown in **Figure 2C** prepared for the formation of conductive traces from a bond pad on the semiconductor wafer to the pad on the glass sheet;

Figure 2E shows the trace formed from the pad on the semiconductor wafer to the pad on the glass sheet;

Figure 2F shows the structure shown in **Figure 2E** with a masking layer formed to allow formation of a solder ball on the pad on the glass sheet;

Figure 2G shows the structure shown in **Figure 2F** with the solder ball formed on the pad on the glass sheet;

Figure 3A shows a cross-section of a portion of the glass sheet shown in **Figure 1A**;

Figure 3B shows the portion of the cross-section of the glass sheet shown in **Figure 3A** with a hole formed in the glass sheet and a pad formed on the surface of the glass sheet with a portion of the pad extending down the sides of the hole in the glass sheet;

Figure 3C shows the cross-section of the glass sheet shown in **Figure 3B** after the glass sheet has been adhered to a semiconductor wafer as shown in **Figure 1C**;

Figure 3D shows the glass sheet/semiconductor wafer structure as shown in **Figure 3C** prepared for the formation of an interconnect material to the pad on the wafer;

Figure 3E shows the structure shown in **Figure 3D** with a masking layer formed to allow formation of a solder ball on the pad on the surface of the glass sheet; and

Figure 3F shows the structure shown in **Figure 3E** with the solder ball formed on the pad on the glass sheet.

DETAILED DESCRIPTION

Reference is now made in detail to specific embodiments of the present invention that illustrate the best mode presently contemplated by the inventor for practicing the invention.

Figures 1A – 1D illustrates how the structure of a glass sheet and semiconductor wafer is formed in accordance with the present invention and a resulting individual chip sawn or cut from the glass sheet/semiconductor wafer structure.

Figure 1A shows a glass sheet **100**. The glass sheet **100** is substantially the same size as the semiconductor wafer to which it will be adhered. The material of the glass sheet is made from a material having a coefficient of expansion that matches the coefficient of expansion of the semiconductor wafer to reduce the stress placed on the wafer due to temperature variations. In addition, the coefficient of expansion of the

glass sheet material can be chosen to also reduce the stress placed on the interconnections to the next level of substrate.

Figure 1B shows the glass sheet **100** with holes **102** etched into and through the glass sheet **100**. It should be appreciated that only a few of the many holes are shown in the surface of the glass sheet **100**. The holes **102** are in a pattern that matches a pattern of bond pads on a semiconductor wafer to which the glass sheet is to be adhered. Also shown are pads **104** formed on the surface of the glass sheet **100** adjacent to the holes **102**. It should also be understood that only a few of the many pads are shown formed on the surface of the glass sheet **100**. The details of the holes **102** and pads **104** are discussed below.

Figure 1C shows the glass sheet **100** adhered to a semiconductor wafer **106** by a layer **108** of adhesive. The glass sheet **100** and layer **108** of adhesive provide electrical insulation from the circuitry on the wafer **106**.

Figure 1D shows the structure shown in **Figure 1C** with the holes **102** filled with a conducting material **110** and solder balls **112** formed on the pads **104**.

Figure 1E shows an individual chip **114** that has been sawn or cut from the glass sheet/semiconductor structure shown in **Figure 1D**. It should be understood that there are many more hole/solder ball structures on an actual chip **114**.

Figures 2A-2G illustrate a method of forming a glass sheet/semiconductor wafer structure according to a first embodiment of the present invention.

Figure 2A shows a cross-section **200** of a portion of the glass sheet **100** shown in **Figure 1A**. **Figure 2B** shows a hole (via) **202** etched through the portion of the

glass sheet **200**. The hole **202** can have tapered sides **204** and **206** or the sides can be non-tapered. The placement of the hole **202** corresponds to a position of a bond pad that is formed on the wafer to which the glass sheet is to be adhered. A pad **208** is formed on the surface of the glass sheet **200** adjacent to each hole **202**. Typically, the pad **208** is formed from a metal such as aluminum or nickel. However, the glass sheet **200** can be pre-metallized with other metals such as gold or copper.

Figure 2C shows the portion of the glass sheet **200** adhered to a portion of a wafer **210** with a layer of adhesive **212**. A metallization pad **214** is shown formed on the surface of the wafer **210**. The layer of adhesive **212** is made from an epoxy that electrically insulates the circuitry on the wafer **210** and, in addition, provides stability to the glass sheet/semiconductor wafer structure. The layer of adhesive **212** conforms to the surface of the semiconductor wafer with or without a passivation layer protecting the semiconductor wafer **210** from the glass sheet **200**. The layer of adhesive **212** is sufficiently compliant to allow a slight mismatch in the coefficient of expansions of the glass sheet **200** and semiconductor wafer **210** thus reducing any stress placed on the semiconductor wafer by a temperature change. The electrical insulation can be increased by increasing the thickness of the glass sheet and/or the thickness of the layer of adhesive **212**. The signal impedance of the device can be controlled by the selection of the glass material for the glass sheet **300**, the selection of the material for the metal pad **308** and by the selection of the layout design parameters.

Figure 2D shows the structure shown in **Figure 2C** with the layer of adhesive over bond pad **214** removed to allow access to the pad **214**. The adhesive over the pad **214** is removed by a plasma etch process.

Figure 2E shows the structure shown in **Figure 2D** with a conductive trace **216** formed that electrically connects pad **208** to the bond pad **214** in the semiconductor wafer **210**. The conductive trace **216** bridges the gap between the glass sheet **200** and the semiconductor wafer **210** created by the thickness of the layer of adhesive **212**. Typically, aluminum is utilized for metallization of bond pads **208** and therefore, deposition of aluminum with an etch removal of excess aluminum is the preferred method of obtaining the bridge metallization. Alternative methods include, but are not limited to a mechanical application of metal such as gold or aluminum, metal plug application in the opening or the use of a conductive polymer such as an epoxy filled with a conductive material such as aluminum flakes. The conductive trace **216** is typically aluminum. Other pad metals may be used and the choice of bridge material and application technique could be varied as appropriate and would be within the skill of a person of ordinary skill in the art. The pre-metallization of the glass sheet **200** allows the use of different metals for the conductive trace **216**, pad **208** and the bond pad **214**. The use of a glass sheet **200** allows the use of a metal for the conductive trace **216** that would otherwise require the use of a diffusion barrier layer between the semiconductor pad **214** and the conductive trace **216** on the glass sheet **200** without having to use a diffusion barrier layer. A typical process would be to metallize the glass with copper or gold and then deposit aluminum in the opening **202**

as the bridge or trace metal. Since aluminum is the most common bond pad material, the use of aluminum as a bridge or trace metal does not adversely affect the bond pad **214** and aluminum is compatible with whatever metal is used as the conductive trace **216**.

Figure 2F shows the structure shown in **Figure 2E** with a mask **218** formed on the surface of the structure shown in **Figure 2E**. A hole **220** is etched in the mask **218** over the pad **208** in order for a solder ball to be formed on the pad **208**.

Figure 2G shows the structure shown in **Figure 2F** with a solder ball **222** formed on the pad **208**. The solder ball **222** allows attachment to a next level of interconnect and is a normal practice for chip scale packages and ball grid array packages. Typically, the solder ball **222** is a tin and lead composition, however, other attachment materials can be used such as a metal bump or a polymer conductive bump.

Figures 3A-3G illustrate a method of forming a glass sheet/semiconductor wafer structure according to a second embodiment of the present invention.

Figure 3A shows a cross-section **300** of a portion of the glass sheet **100** shown in **Figure 1A**. **Figure 3B** shows a hole (via) **302** etched through the portion of the glass sheet **300**. The hole **302** can have tapered sides **304** and **306** as shown or the sides can be non-tapered. The placement of the hole **302** in the glass sheet **300** corresponds to a position of a pad that is formed on the wafer to which the glass sheet is to be adhered. A metal pad **308** is formed on the surface of the glass sheet **300** and on the sides **304** and **306** of the hole **302**. A metal pad **308** is formed as shown for

each hole **302**. Typically, the metal pad **308** is formed from a metal such as aluminum or nickel. However, the pad **308** can be formed from other metals such as gold or copper.

Figure 3C shows the portion of the glass sheet **300** adhered to a portion of a wafer **310** with a layer of adhesive **312**. A bond pad **314** is shown formed on the surface of semiconductor wafer **310**. The layer of adhesive **312** is an epoxy that electrically insulates the circuitry on the wafer **310** and, in addition, provides stability to the glass sheet/semiconductor wafer structure. The layer of adhesive **312** conforms to the surface of the semiconductor wafer with or without a passivation layer protecting the wafer **310** from the glass sheet **300**. The layer of adhesive **312** is sufficiently compliant to allow slight mismatch in the coefficient of expansions of glass sheet **200** and semiconductor wafer **310** thus reducing any stress placed on the semiconductor wafer by a temperature change. The electrical insulation can be increased by increasing the thickness of the glass sheet and/or the thickness of the layer of adhesive **312**. The signal impedance of the device can be controlled by the selection of the glass material for the glass sheet **300**, the selection of the material for the metal pad **308** and by the selection of the layout design parameters.

Figure 3D shows the structure shown in **Figure 3C** with the layer of adhesive over the pad **314** removed to allow access to the bond pad **314**. The adhesive over the bond pad **314** is removed by a plasma etch process.

Figure 3E shows the structure shown in **Figure 3D** with a metal plug **316** formed in the hole **302**. The metal plug **316** electrically connects pad **308** to bond pad

314 in the semiconductor wafer **310**. The metal plug **316** bridges the gap between the glass sheet **300** and the wafer **310** created by the thickness of the layer of adhesive **312**. Typically, aluminum is utilized for metallization of bond pads **308** and therefore, deposition of aluminum with an etch removal of excess aluminum is the preferred method of obtaining the plug metallization. Alternative methods include, but are not limited to a mechanical application of metal such as gold or aluminum or the use of a conductive polymer such as an epoxy filled with a conductive material such as aluminum flakes. Other applications may utilize other pad metals and the choice of a plug material and application technique could be varied as appropriate and would be within the skill of a person of ordinary skill in the art. The pre-metallization of the glass sheet **300** allows use of different metals for the metal plug **316**, pad **308** and the metal trace **316**. The use of glass sheet **300** allows the use of a metal for the conductive plug **316** that would otherwise require the use of a diffusion barrier layer between the bond pad **314** and the metal pad **308** on the glass sheet **300** without having to use the diffusion barrier layer. A typical process, in this case, would be to metallize the glass with copper or gold and then deposit aluminum in the opening **302** as the plug material. Since aluminum is the most common bond pad material, the use of aluminum as the plug material does not adversely affect the bond pad **314** and aluminum is compatible with whatever metal is used as the metal pad **308**.

Figure 3F shows the structure shown in **Figure 3E** with a mask **318** formed on the surface of the structure shown in **Figure 3E**. A hole **320** is etched in the mask **318** over a portion of the pad **308** in order for a solder ball to be formed on the pad **318**.

Figure 3G shows the structure shown in **Figure 3F** with a solder ball **322** formed on the pad **308**. The solder ball **322** allows attachment to a next level of interconnect and is a normal practice for chip scale packages and ball grid array packages. Typically, the solder ball **322** is a tin and lead composition, however, other attachment materials can be used such as a metal bump or a polymer conductive bump.

In summary, the results and advantages of the chip scale structures of the present invention can now be more fully realized. The use of one glass sheet is easy to implement and is less costly than the current methods of producing chip scale packages.

The foregoing description of the embodiments of the invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed. Obvious modifications or variations are possible in light of the above teachings. The embodiments were chosen and described to provide the best illustration of the principles of the invention and its practical application to thereby enable one of ordinary skill in the art to utilize the invention in various embodiments and with various modifications as are suited to the particular use contemplated. All such modifications and variations are within the scope of the invention as determined by the appended claims when interpreted in accordance with the breadth to which they are fairly, legally, and equitably entitled.

CLAIMS

What is claimed is:

1. A chip scale structure comprising:

a semiconductor wafer with a pattern of bond pads on the surface of the semiconductor wafer;

a glass sheet with holes in a pattern matching the pattern of bond pads on the surface of the semiconductor wafer; and

a layer of adhesive adhering the glass sheet to the semiconductor wafer wherein the pattern of holes in the glass sheet are over the pattern of bond pads on the surface of the semiconductor wafer.

2. The chip scale structure of Claim 1 further comprising a metallized pad formed on the glass sheet adjacent to each hole in the glass sheet.

3. The chip scale structure of Claim 2 further comprising a conductive trace connecting each metallized pad on the glass sheet to a corresponding bond pad on the surface of the semiconductor wafer under the hole adjacent to the metallized pad on the glass sheet.

4. The chip scale structure of Claim 3 further comprising a solder ball formed on each metallized pad on the glass sheet.

5. The chip scale structure of Claim 1 further comprising a metallized pad formed on the glass sheet adjacent to each hole in the glass sheet wherein the metallized pad extends down sides of the hole adjacent to the metallized pad.

6. The chip scale structure of Claim 5 further comprising a metal plug formed in each hole connecting the metallized pad on the sides of each hole to the bond pad under each hole.

7. The chip scale structure of Claim 5 further comprising a solder ball formed on each metallized pad on the glass sheet.

8. A method of forming a chip scale structure, the method comprising:

forming a pattern of holes in a glass sheet wherein the pattern of holes in the glass sheet matches a pattern of bond pads on a surface of a semiconductor wafer; and

adhering the glass sheet to the semiconductor die wherein the pattern of holes in the glass sheet are over the pattern of bond pads on the semiconductor wafer.

9. The method of Claim 8 further comprising forming a metallized pad on the surface of the glass sheet adjacent to each hole in the glass sheet.

10. The method of Claim 9 further comprising forming a conductive trace connecting each metallized pad on the glass sheet to the bond pad on the surface of the semiconductor wafer under the hole adjacent to the metallized pad on the glass sheet.

11. The method of Claim 10 further comprising forming a solder ball formed on each metallized pad on the glass sheet.

12. The method of Claim 8 further comprising forming a metallized pad on the glass sheet adjacent to each hole in the glass sheet wherein the metallized pad extends down sides of the hole adjacent to the metallized pad.

13. The method of Claim 12 further comprising forming a metal plug formed in each hole connecting the metallized pad on the sides of each hole to the bond pad under each hole.

14. The method of Claim 13 further comprising forming a solder ball on each metallized pad on the glass sheet.

CHIP SCALE PACKAGES

Donald Malcolm MacIntyre

ABSTRACT

A chip scale package structure formed by adhering a glass sheet having a pattern of holes matching a pattern of bond pads on a semiconductor wafer so that the pattern of holes on the glass sheet are over the pattern of bond pads on the semiconductor wafer. Metallized pads are formed on the glass sheet adjacent to each hole and in one embodiment a conductive trace is formed from each metallized pad on the glass sheet to the bond pad on the semiconductor wafer under the adjacent hole. In a second embodiment, a pad is formed on the glass sheet adjacent to each hole and the pad extends down the sides of the adjacent hole. The hole is filled with a metal plug that electrically connects the pad on the glass sheet to the bond pad on the semiconductor wafer. In each embodiment, a solder ball is formed on each pad on the glass sheet.

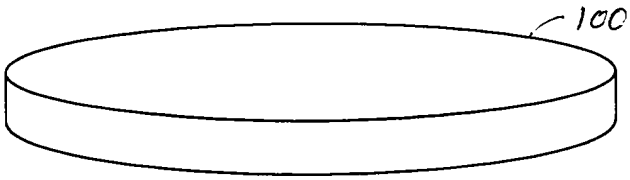

FIGURE 1A

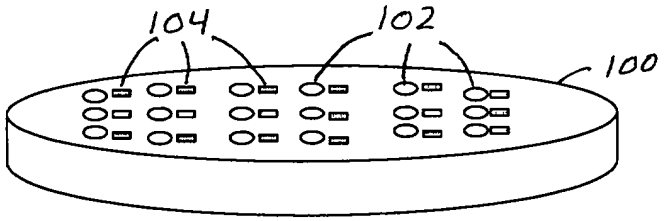

FIGURE 1B

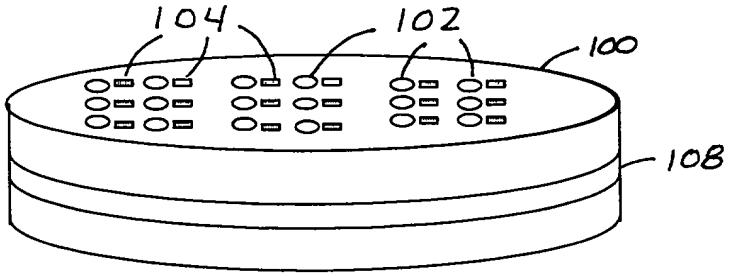

FIGURE 1C

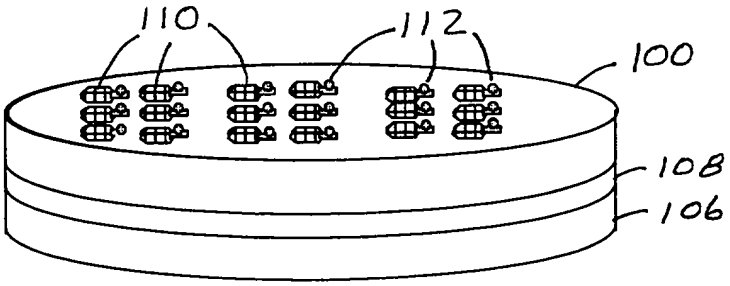

FIGURE 1D

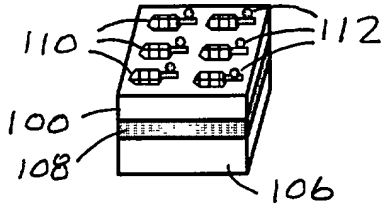

FIGURE 1E

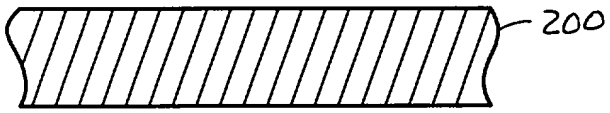

FIGURE 2A

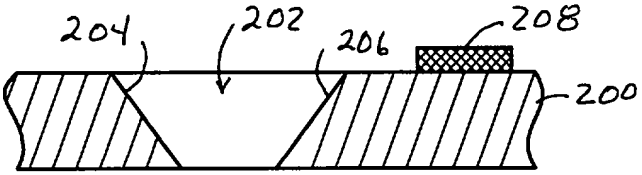

FIGURE 2B

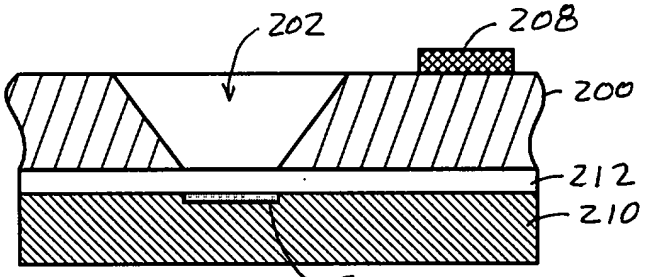

FIGURE 2C

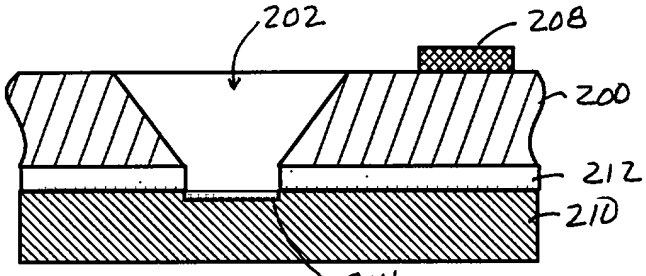

FIGURE 2D

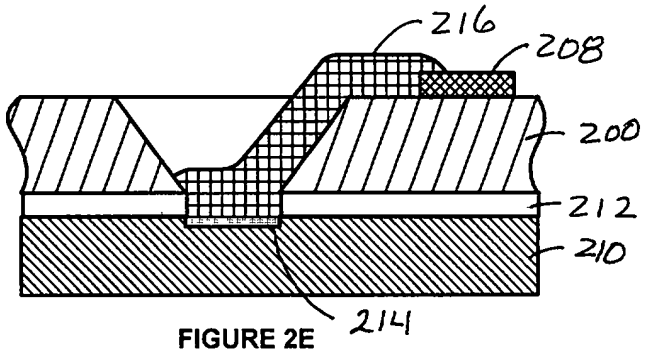

FIGURE 2E

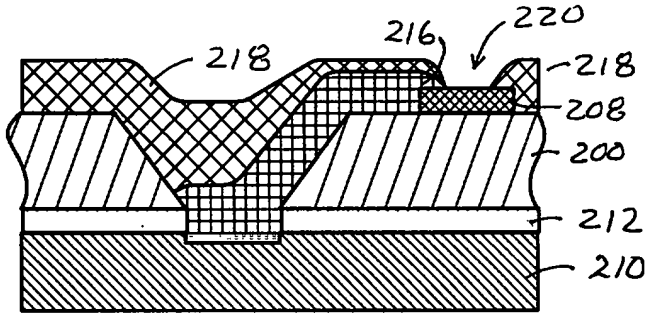

FIGURE 2F

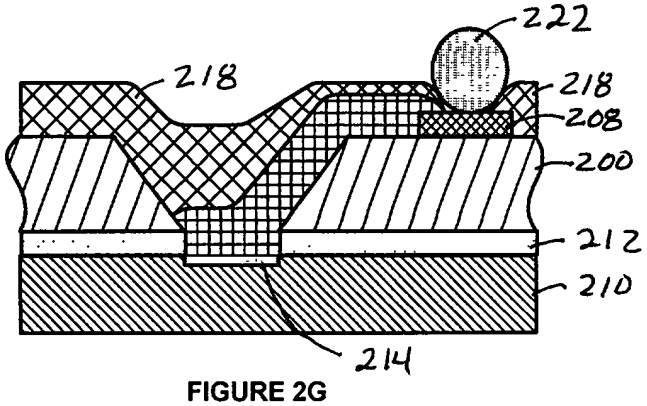

FIGURE 2G

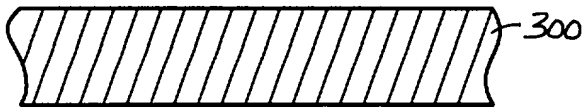

FIGURE 3A

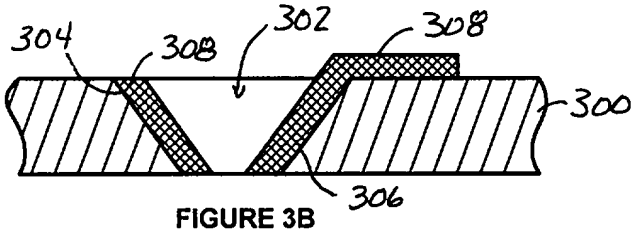

FIGURE 3B

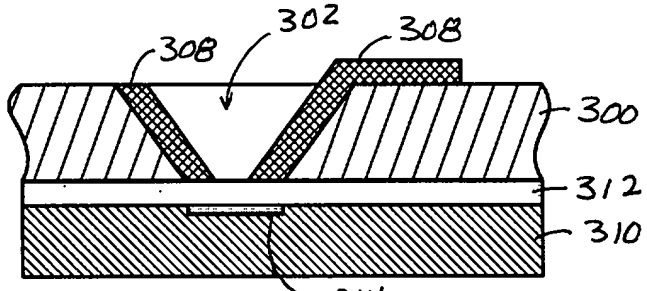

FIGURE 3C

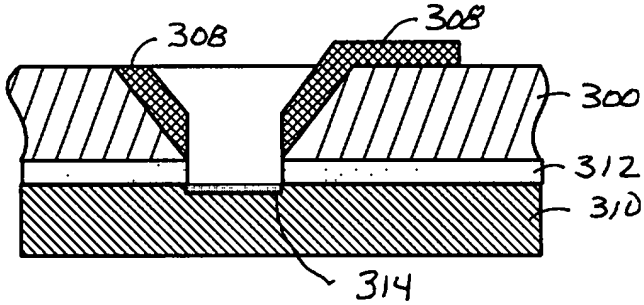

FIGURE 3D

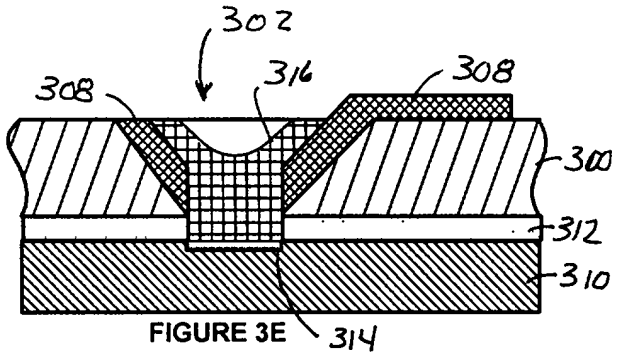

FIGURE 3E

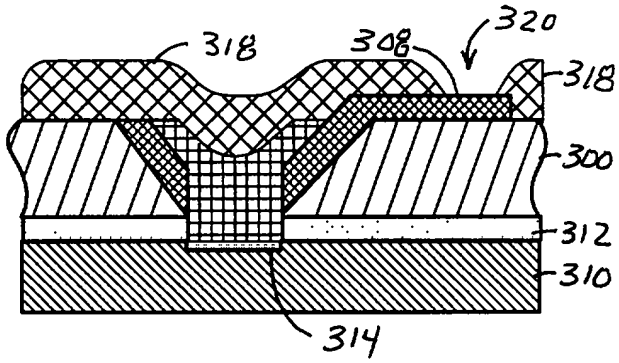

FIGURE 3F

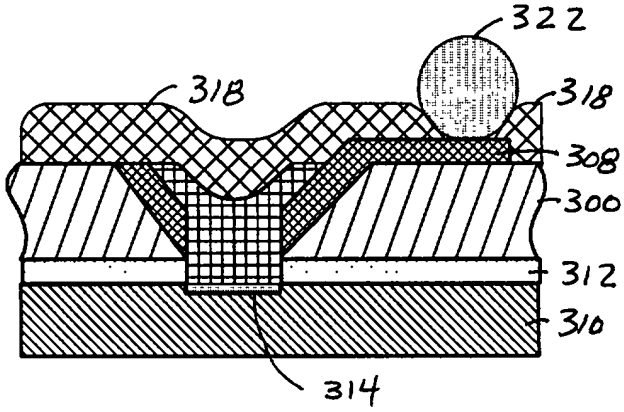

FIGURE 3G

Docket No.
MAI1003

Declaration and Power of Attorney For Patent Application

English Language Declaration

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

CHIP SCALE PACKAGES

the specification of which

(check one)

☒ is attached hereto.

☐ was filed on _____ as United States Application No. or PCT International Application Number _____

and was amended on _____

(if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d) or Section 365(b) of any foreign application(s) for patent or inventor's certificate, or Section 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)			Priority Not Claimed
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	☐
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	☐
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	☐

I hereby claim the benefit under 35 U.S.C. Section 119(e) of any United States provisional application(s) listed below:

(Application Serial No.)	(Filing Date)

I hereby claim the benefit under 35 U. S. C. Section 120 of any United States application(s), or Section 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. Section 112, I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, C. F. R., Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(list name and registration number)*

H. Donald Nelson, Reg. No. 28,980

Send Correspondence to: **H. Donald Nelson**
5492 Livorno Court
San Jose, CA 95138

Direct Telephone Calls to: *(name and telephone number)*
Don Nelson (408) 239-0225

Full name of sole or first inventor **Donald Malcolm MacIntyre**
Sole or first inventor's signature Donald Malcolm MacIntyre Date March 26, 1998
Residence **San Jose, California**
Citizenship **USA**
Post Office Address **P.O. Box 641686**
San Jose, CA 95164

Full name of second inventor, if any
Second inventor's signature Date
Residence
Citizenship
Post Office Address

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS (37 CFR 1.9(f) AND 1.27 (b)) - INDEPENDENT INVENTOR	Docket No. MAI1003

Serial No.	Filing Date	Patent No.	Issue Date

Applicant/ Patentee: **Donald Malcolm MacIntyre**

Invention: **CHIP SCALE PACKAGES**

As a below named inventor, I hereby declare that I qualify as an independent inventor as defined in 37 CFR 1.9(c) for purposes of paying reduced fees under section 41(a) and (b) of Title 35, United States Code, to the Patent and Trademark Office with regard to the invention entitled above and described in:

- ☒ the specification to be filed herewith.
- ☐ the application identified above.
- ☐ the patent identified above.

I have not assigned, granted, conveyed or licensed and am under no obligation under contract or law to assign, grant, convey or license, any rights in the invention to any person who could not be classified as an independent inventor under 37 CFR 1.9(c) if that person had made the invention, or to any concern which would not qualify as a small business concern under 37 CFR 1.9(d) or a nonprofit organization under 37 CFR 1.9(e).

Each person, concern or organization to which I have assigned, granted, conveyed, or licensed or am under an obligation under contract or law to assign, grant, convey, or license any rights in the invention is listed below:

- ☒ No such person, concern or organization exists.
- ☐ Each such person, concern or organization is listed below.

*NOTE: Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities (37 CFR 1.27)

FULL NAME _____

ADDRESS _____

☐ Individual ☐ Small Business Concern ☐ Nonprofit Organization

FULL NAME _____

ADDRESS _____

☐ Individual ☐ Small Business Concern ☐ Nonprofit Organization

FULL NAME _____

ADDRESS _____

☐ Individual ☐ Small Business Concern ☐ Nonprofit Organization

FULL NAME _____

ADDRESS _____

☐ Individual ☐ Small Business Concern ☐ Nonprofit Organization

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b))

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

NAME OF INVENTOR **Donald Malcolm MacIntyre**
SIGNATURE OF INVENTOR Donald Malcolm MacIntyre DATE: March 20, 1998

NAME OF INVENTOR ______
SIGNATURE OF INVENTOR ______ DATE: ______

NAME OF INVENTOR ______
SIGNATURE OF INVENTOR ______ DATE: ______

NAME OF INVENTOR ______
SIGNATURE OF INVENTOR ______ DATE: ______

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NAME OF INVENTOR ______
SIGNATURE OF INVENTOR ______ DATE: ______